Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1. (Canceled)

2. (New) A first-in-first-out circuit comprising:

a write pointer circuit coupled to receive a write clock signal and configured to generate a plurality of mutually exclusive write pointer signals in accordance with the write clock signal;

a read pointer circuit coupled to receive a read clock signal and configured to generate a plurality of mutually exclusive read pointer signals in accordance with the read clock signal; and

a plurality of registers coupled to receive an input signal, the registers configured to store data from the input signal in accordance with the write pointer signals and configured to output data in accordance with the read pointer signals.

3. (New) The first-in-first-out circuit of claim 2 wherein each of the registers is configured to receive a unique one of the write pointer signals from the write pointer circuit.

4. (New) The first-in-first-out circuit of claim 3 wherein each of the registers is configured to receive a unique one of the read pointer signals from the read pointer circuit.

5. (New) The first-in-first-out circuit of claim 2 wherein each of the registers is configured to receive a unique one of the read pointer signals from the read pointer circuit.

6. (New) The first-in-first-out circuit of claim 2 wherein the write pointer circuit comprises a plurality of flip-flops serially coupled in a ring.

7. (New) The first-in-first-out circuit of claim 2 wherein the read pointer circuit comprises a plurality of flip-flops serially coupled in a ring.

8. (New) The first-in-first-out circuit of claim 2 comprising an output register coupled to receive the data output by the registers and configured to output data in accordance with the read clock signal.

9. (New) The first-in-first-out circuit of claim 2 comprising a fifo pointer control circuit configured to generate signals for controlling the write pointer circuit and the read pointer circuit.

10. (New) The first-in-first-out circuit of claim 9 wherein the fifo pointer control circuit is configured to receive

control signals to generate the signals for controlling the write pointer circuit and the read pointer circuit.

11. (New) The first-in-first-out circuit of claim 10 wherein the control signals comprise at least one of a lock detect signal, a pointer reset signal, the write clock signal and the read clock signal.

12. (New) A method of synchronizing received data comprising:

receiving an input signal;

receiving a write clock signal associated with the input signal;

generating a plurality of mutually exclusive write pointer signals in accordance with the write clock signal;

storing data from the input signal into a plurality of registers using the write pointer signals;

receiving a read clock signal;

generating a plurality of mutually exclusive read pointer signals in accordance with the read clock signal; and

reading data stored in the registers using the read pointer signals.

13. (New) The method of claim 12 wherein each of the registers is configured to receive a unique one of the write pointer signals.

14. (New) The method of claim 13 wherein each of the registers is configured to receive a unique one of the read pointer signals.

15. (New) The method of claim 12 wherein each of the registers is configured to receive a unique one of the read pointer signals.

16. (New) The method of claim 12 wherein the write pointer signals are generated by a plurality of flip-flops serially coupled in a ring.

17. (New) The method of claim 12 wherein the read pointer signals are generated by a plurality of flip-flops serially coupled in a ring.

18. (New) The method of claim 12 comprising generating an output data signal from the read data in accordance with the read clock signal.

19. (New) The method of claim 12 comprising receiving control signals to control the generation of the write pointer signals and the read pointer signals.

20. (New) The method of claim 19 wherein the control signals comprise at least one of a lock detect signal, a pointer reset signal, the write clock signal and the read clock signal.